Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to further clarify Applicants invention. No new matter has been added.

For example support for the amendments is found in the previously presented claims, in the Figures including Figure 2C, and in the Specification including at:

Beginning at line 13, page 18:

"Referring to Figure 2C, following the selective radiant energy exposure and development process to improve a planarity of the process surface, an etchback process is carried out to etch back the resist layer 28, for example by a conventional oxygen containing dry etching process to form Vias at least partially filled with resist plugs e.g., 28A, 28B, 28C, 28D, and 28E, **preferably formed at about the same level**, for example about a level equal to the depth of a subsequently formed overlying trench. It will be appreciated that the selectively controlled radiant energy exposure method of the present invention advantageously results in **a more uniform height of Via plugs over the process wafer surface following the etchback process** thereby improving an etching profile in a subsequent overlying trench etching process while avoiding the formation of Via fences formed of etching resistant residues."

Claim Rejections under 35 USC 103

1. Claims 1, 2, 4-8, 10-13, 15-19, and 25-31 stand rejected under 35 USC 102(b) as being anticipated by Sato (US 6,064,466) in view of Beyer (US (US 4,333,794).

Sato discloses a method for selectively exposing a resist layer over a **single feature** (protruding or indented) or a plurality of trenches **(having a uniform density)** (see Figures 4, 5, and 7) (Figure 7; col 4, lines 62 - col 5, line 14) to form a planarized resist layer (Figure 7(c) item 44 or to form resist **partially filling trenches** (item 45) (see Abstract; col 3, lines 1-14; col 3, lines 65-67; col 4, lines 19-22; col 4, lines 45-47; col 4, lines 62-66; col 5, lines 15-18; Figures 4-7).

Sato discloses that the amount of light falling on the resist overlying the **single feature** may be adjusted by a mask having at least three different light transmittance portions (Figure 4, col 3, lines 15-20) where the light transmittance portions in the mask **are determined by the pattern density in the mask** (see col 1, lines 48-53; col 3, lines 35-40). To adjust the amount of resist removed over the **single features or multiple**

features having a single density to achieve a planar surface, the **mask variable pattern density portions is aligned in a desired manner** over the single or multiple features (having a single density) (**i.e., high and medium density of the mask pattern aligned over sidewalls in the case of a protruding single feature**) (col 3, lines 47-62) or (low density mask pattern portions (high transmittance) aligned over the thick part of the resist and high density pattern portions aligned over the thin part of the resist (col 5, lines 1-14) to adjust the amount of exposure of the resist.

Sato **shows schematically** in the Figures (see Figures 4(d), 4(e), 7(c)) the difference between the **original resist layer thickness** and the amount left after exposure and development.

Nowhere does Sato disclose (inherently or explicitly) a step of **measuring** the thickness of the resist or disclose or suggest semiconductor features having a first and a second density.

Thus Sato fails to disclose several aspects of Applicants disclosed and claimed invention including:

With respect to claim 1, Sato does not disclose the

following aspects of Applicants invention including those in **bold type:**

"A method for selectively planarizing a radiation sensitive polymer layer to **improve a subsequent etchback process"**

forming at least one radiation sensitive polymer layer having a first thickness topography to cover said semiconductor features;

measuring a thickness of the first thickness topography;

determining a radiant energy transmittance distribution **based on said measured first thickness topography to produce a second thickness topography;**

exposing the at least one radiation sensitive polymer layer through a mask having said determined radiant energy transmittance distribution **to selectively expose said polymer layer over said second density of semiconductor features to a different radiant energy dosage compared to said polymer layer over said first density of semiconductor features;**

developing the at least one radiation sensitive polymer layer in said development process to produce said second thickness topography wherein said second thickness topography covers said semiconductor features and has a higher degree of planarity than said first thickness topography; and,

performing an etchback process of said second thickness topography to produce a third thickness topography having substantially uniform thickness."

Applicants respectfully suggest Examiner is mistaken that Sato anywhere refers to or suggests semiconductor features having a first and a second density. Rather, as pointed out above, Sato refers to **three different pattern densities of a mask**. Examiner apparently argues that since Sato shows multiple trenches next to a planar wafer surface (see Fig 7(c)) that "this equates to a low pattern density over the non-trenched region and a high pattern density over the trenched region (i.e., first and second density)". Examiner also refers to Figure 7 (b). Applicants respectfully suggest that Sato is referring **to the pattern density of the mask** (see col 5, lines 1-14, especially lines 7-10). Figure 7(b) is referring to an increasing pattern density of the mask **(not semiconductor feature density)** (see col 5, lines 1-

2). Applicants respectfully suggest that there is no teaching in Sato that would be understood by one of ordinary skill in the art as disclosing "a first density of semiconductor features and a second density of semiconductor features **wherein said first density is greater than said second density**" as Applicants have disclosed and claimed. **As noted, Sato only refers to single and multiple semiconductor features having a single density.**

Sato additional fails to disclose the step of:

"measuring a thickness of the first thickness topography;

determining a radiant energy transmittance distribution **based on said measured first thickness topography to produce a second thickness topography;**"

Sato nowhere discusses (inherently or explicitly) **measuring** the thickness of the photoresist or a thickness topography of the photoresist (including over a first density and a second density of semiconductor features), or discloses a method of **measuring** the thickness, or when such thickness is **measured.** Rather, Sato **merely shows different thickness (between planar and non-planar resists layers in phantom) over the features for explanatory**

purposes.

Examiner argues that "it is inherent that if one is to planarize a layer that the thickness of that layer must be determined before planarization or too much material might be removed. Examiner also argues "that this thickness can also be determined which the resist is first applied by a spin speed". Examiner has cited no support for the above assertions. Sato et al. nowhere discloses any such measurement process, but rather infers a different thickness based on the density of the features and the fact that **resist flows into the trenches** (see col 4, lines 62-67).

"To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *In re Oelrich, 666 F.2d 578, 581-582, 212 USPQ 323, 326 (CCPA 1981).*

"In relying on the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent

characteristic *necessarily* flows from the teachings of the applied prior art." *Ex Parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)*

Nevertheless, Sato nowhere discloses or suggests:

"determining a radiant energy transmittance distribution **based on said measured first thickness topography to produce a second thickness topography;**"

In addition, Sato further does not suggest or disclose:

performing an etchback process of said second thickness topography to produce a third thickness topography having substantially uniform thickness."

Rather, Sato specifically teaches performing photoresist exposure and development to produce a planarized surface including photoresist within a trench below the upper surface of the trench (col 5, lines 13-19).

With respect to claim 15, Sato nowhere discloses vias or the formation of vias. Rather Sato refers to "pits" and only teaches

reducing the level of resist on either side of the pit to be equalized (co-planar) with the semiconductor substrate (col 4, lines 16-22).

Sato also nowhere discloses or suggests Applicants steps of:

"providing a semiconductor wafer having a process surface comprising **a first density of via openings and a second density of via openings formed in a dielectric layer, said first density greater than said second density;**"

or

"**measuring** a thickness topography of the radiation sensitive polymer layer;

"**determining a desired radiant energy dosage based on said measured first thickness topography** to deliver to portions of the radiation sensitive polymer layer **to produce a subsequent planarized thickness topography** of the radiation sensitive polymer layer;

or

"selectively exposing portions of the radiation sensitive polymer layer through the exposure mask to deliver the desired radiant energy dosage **including a relatively higher radiant energy dosage to an area of said polymer layer overlying said second density**"

or

developing the radiation sensitive polymer layer in said development process to produce the subsequent planarized thickness topography wherein said planarized thickness topography comprises a thickness portion above and **covering said via openings**; and,

performing an etchback process of said planarized thickness topography to form via plugs at a substantially uniform height within said via openings."

On the other hand Beyer discloses a method of forming a **bipolar transistor** where a **polysilicon etchback process** is used to form portions of the emitter (see Abstract; col 10, lines 43-

61; col 1, lines 1-15). Beyer also discloses **forming a resist plug by etching back a nonplanar resist layer** to protect a 1 micron deep trench **formed during etching back of an SiO2 layer** (col 10, lines 43-48).

There is no apparent motivation for combining the method of Sato with the method of Beyer. Sato nowhere suggests that an etchback process could be used to form a resist level within trenches (or vias) and Beyer nowhere discloses or suggests a resist planarization process prior to etchback. The fact that etchback processes, in general, are conventionally used in several different types of processes does not provide Examiner with a proper motivation for combination.

Moreover, using the etchback process of Beyer to further planarize a resist layer in the method of Sato form the trench levels (45; Fig 7(c)) of Sato would likely etchback the wafer surface of Sato (i.e., the etchback process of Beyer simultaneously etches SiO2) and make the method of Sato unsuitable for its intended purpose.

Even assuming *arguendo*, a proper motivation for combination, such combination does not produce Applicants disclosed and

claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Finally, when evaluating the scope of a claim, every limitation in the claim must be considered. Office personnel may not dissect a claimed invention into discrete elements and then evaluate the elements in isolation. Instead, the claim as a whole must be considered. See, e.g., *Diamond v. Diehr*, 450 U.S. at 188-189, 209 USPQ at 9.

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

Moreover, the combined teachings of Sato and Beyer do not

recognize or provide a solution to the problem that Applicants have disclosed and solved.

"A method for selectively planarizing a radiation sensitive polymer layer to improve a subsequent etchback process"

Examiner argues that the prior art does not have to solve the same problem as the current Application. While Examiner may be correct in this assertion, the prior art does have to provide a motivation to do what Applicants have done, which the prior art does not provide, and which as explained above, the non-analogous etchback process of Beyer (not a planarization process) would change the principle of operation of the planarization process (resist exposure and development) of Sato.

"[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103." *In re Sponnoble*, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969).

2. Claim 3 stands rejected under 35 USC 103(a) as being unpatentable over Sato in view of Beyer, above, and further in view of Lewis (US 4,822,722).

Applicants reiterate the comments made above with respect to Sato and Beyer.

Even assuming arguendo a proper motivation for combination, the fact that Lewis teaches that the thickness of a photoresist layer **following development** may be measured using interferometry, profilometry or ellipsometry, does not further help Examiner in producing Applicants disclosed and claimed invention. See. e.g., at col 6, lines 34-44:

"Following development, the workpiece can be rinsed with water and further processed in a conventional manner. The thickness of the photoresist remaining can be measured by any suitable method, such as interferometry, profilometry and elipsometry."

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

3. Claim 14 stands rejected under 35 USC 103(a) as being unpatentable over Sato, above, and further in view of Aronsatein (US 3,889,355).

Even assuming *arguendo*, a proper motivation for combination, the fact that Aronsatein discloses various methods of resist exposure including **using a mask from a mask library** (col 10, lines 25-27) in an unrelated process, does not further help Examiner in producing Applicants invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

The cited references, either singly or in combination, fail to produce or suggest Applicants disclosed and claimed invention

and therefore fail to make out a *prima facie* case of obviousness.

The Claims have been amended to further clarify Applicants' disclosed and claimed invention. A favorable consideration of Applicants' claims is respectfully requested.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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